REMARKS

This paper is responsive to a Non-Final Office action dated July 18, 2006. Claims 1-23 were examined.

Applicant appreciates the courtesy extended during the telephone interview with the Examiner on October 17, 2006 in which the claim rejections under 35 U.S.C. § 112, first paragraph, for claims 19-21 were discussed. The Examiner also confirmed that the art rejection for claims 1-9 and 11-23 was under 35 U.S.C. §102(b). Applicant further appreciates the interview with Examiner Fleming on October 19, in which the claim rejections under 35 U.S.C. § 112, first paragraph, were discussed. The applicant's position is presented below.

Claim Rejections Under 35 U.S.C. § 112

Claims 19-21 are rejected under 35 U.S.C. § 112, first paragraph, because the specification does not reasonably provide enablement for those structures not known by the inventor because the Office action maintains that claim 19 is a single means claim. Applicant respectfully requests reconsideration of the rejection in view of the following.

35 U.S.C. § 112, paragraph 6, states that "[a]n element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. § 112, paragraph 6 (emphasis added). The Federal Circuit discusses § 112, paragraph 6 as follows:

> The final paragraph of Sec. 112 saves combination claims drafted using means-plus-function format from [the overbreadth] problem by providing a construction of that format narrow enough to avoid the problem of undue breadth as forbidden by the first paragraph. But no provision saves a claim drafted in means-plus-function format which is not drawn to a combination, i.e., a single means claim.

In Re Hyatt, 708 F.2d 712, 715, (Fed. Cir. 1983) (emphasis added). However, Hyatt also states that attempts to evade a single means rejection "by adding purely nominal elements to such a claim will undoubtedly be condemned." Hyatt, at 713-714.

Applicant points out that claim 19 includes two elements: (1) a terminal and (2) a means for permanently converting the terminal. Thus, the means recitation does appear in combination with another recited element and meets the requirements of 35 U.S.C. § 112, sixth paragraph. Further, applicant submits that the non-means element is not merely a nominal element. Thus, applicant respectfully submits that claim 19 is not a single means element under the statute and case law and reconsideration of the rejection is respectfully requested.

Applicant notes that claim 20 recites another element (non-volatile memory) that is not merely a nominal element and thus has three elements in combination.

In view of the above, applicant respectfully requests that the rejection of claims 19-21 under 35 U.S.C. § 112, first paragraph, be reconsidered and withdrawn.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-9 and 11-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by U. S. Patent No. 5,451,912 to Torode (hereinafter, "Torode").

Claim 1

Claim 1 recites *control circuitry coupled to the terminal to permanently convert the terminal from a first mode of operation in which serial communications are received over the terminal into a second mode of operation in which the terminal functions to selectively enable an output according to a voltage value on the terminal.* The Office action maintains in paragraph 4 that Torode teaches that "the mode change from the first mode to the second mode is permanent as apparatus programming is a one time event" and "that the storage used for programming is only programmable once." The Office action maintains that "[o]nce the device [in Torode] is programmed, there is no way to program it again and therefore there is no need to return to the programming mode once programmed."

Applicant respectfully maintains that Torode fails to teach *permanently converting the terminal from a first mode of operation in which serial communications are received over the terminal into a second mode of operation in which the terminal functions to selectively enable an output*. Even if Torode teaches programming the memory once, that fails to teach permanently converting the terminal from the first to second mode of operation as claimed. The lack of a need to return to the programming mode is not a teaching of permanently converting the terminal to the second mode of operation. There may be other reasons, e.g., test and diagnostic operations, that would make one want to maintain a serial communication capability regardless of whether programming is available. "A single prior art reference anticipates a patent claim if it expressly or inherently describes each and every limitation set forth in the patent claim." Trintec Indus., Inc. v. Top-U.S.A. Corp., 295 F.3d 1292; 63 USPQ2d 1597 (Fed. Cir. 2002) (citing Verdegaal Bros. v. Union Oil Co. of Cal., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Torode simply does not teach the mode change is permanent. Even if there is no need to return to the programming mode once programmed in Torode, Torode fails to teach *permanently converting the terminal.*

Applicant still maintains that instead of teaching *permanently converting* as claimed, Torode, in fact, teaches that the OD pin is always capable of receiving serial input data. Torode teaches that the shift register 710 in Fig. 7 continually shifts data when the programmable crystal oscillator 100 is powered on. Col. 6, lines 28-30. On detection of a start bit, the shift register shifts in serial data. Col. 6, lines 30-32. In all the description of the use of the OD pin as the serial input, nowhere does Torode discuss permanently disabling the shift register 710. In fact, Torode says that the stop shift logic 720 disables the shift register by deactivating the shift output after the 28 bit input parameter has been received. Col. 6, lines 43-48. Torode teaches in col. 7 that the power on initialization circuit 75 clears the shift register and that power needs to be cycled each time the programming circuit is to receive a new input parameter.

While applicant agrees that Torode teaches that power cycling is necessary for programming, there is nothing teaching that the circuitry that clears the shift register on power on initialization is somehow disabled after programming. In fact, Torode teaches at col. 6 lines 28-34:

> The shift register continuously shifts data when the programmable crystal oscillator 100 is powered on. However, upon detection of a start bit, which signifies the beginning of input parameter data, the shift register 710 shifts in the serial data parameter, and subsequently converts the serial data parameter into 28 bits of parallel data.

There is no ambiguity about the underlined statement. While Torode may teach one time programming, Torode does not teach anywhere permanently converting the OD pin and, in fact, explicitly teaches that the shift register and, hence, the OD pin is not ever converted to not operate as a serial input. The fact that Torode may teach one time programming is simply not dispositive of the issue.

The Office action rebuts the applicant's arguments that Torode does not teach permanently changing modes with respect to the terminal by stating that the claims do not require a permanent mode change in view of the specification. Applicant notes that claim 1 recites *permanently convert[ing] the terminal from a first mode of operation in which serial communications are received over the terminal into a second mode of operation in which the terminal functions to selectively enable an output according to a voltage value on the terminal.* Each and every claim limitation must be given weight. Applicant's specification in no way redefines "permanently converting". The Office action points to an embodiment in which NVM may be written twice, suggesting that implies that the mode change is not permanent on the terminal. Applicant maintains that the number of times the NVM is written is just not relevant to the operational mode of the terminal. That is made explicitly clear in paragraph 1032, which provides an embodiment having a P1 pin that is a dedicated I/O pin along with a P2 pin that can be permanently converted. In fact, that embodiment is even claimed in claim 10 in which a second terminal is provided that functions as a dedicated programmable input/output terminal that is not convertible. Thus, the number of times that the NVM can be programmed is irrelevant. Applicant respectfully submits that the Examiner's position regarding refusing to give appropriate weight to *permanently converting* is improper.

In view of the above, applicant respectfully submits that claim 1 and all claims dependent thereon distinguish over the references of record.

Claim 11

Amended claim 11 recites *permanently converting the terminal to a second mode of operation in response to a received command, in which the terminal functions as an input control for selectively enabling an output according to a value of terminal voltage, the second mode of operation permanently disabling the first mode of operation.* The Office action states that Torode teaches the mode change is permanent. Applicant disagrees for similar reasons as set forth in the discussion of claim 1. The fact that storage in Torode is used for one time programming does not mean that the terminal ceases to function in the serial communications mode; it just means that programming through the terminal is not available.

Claim 19

Claim 19 recites means for permanently converting the terminal from a first mode of operation in which serial communications are received over the terminal into a second mode of operation in which the terminal functions as a control input to selectively enable an output according to a voltage value on the terminal. As Torode fails to teach "means for permanently converting" for reasons set forth above, applicant submits that claim 19 and all claims dependent thereon distinguish over the references of record.

Claim 10

Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Torode in view of U. S. Patent No. 6,664,860 to Fallisgaard (hereinafter, "Fallisgaard"). The Office action states that Fallisgaard teaches a dedicated programming input, and one would be motivated to modify the teachings of Torode to include the dedicated programming input. However, Torode teaches that an object of his invention is to provide a programmable crystal oscillator that does not require any dedicated programming connections. See col. 1, lines 64-66. Thus, Torode teaches away from any combination incorporating a dedicated programming pin, rendering the combination of Torode and Fallisgaard improper. See MPEP §2145(X)(D). Accordingly, applicant submits that claim 10 distinguishes over the art of reference.

In summary, claims 1-11 and 12-23 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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